

Fig. 1

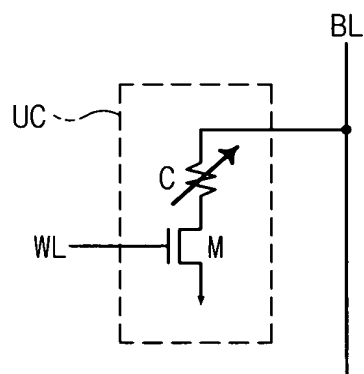


Fig. 2A

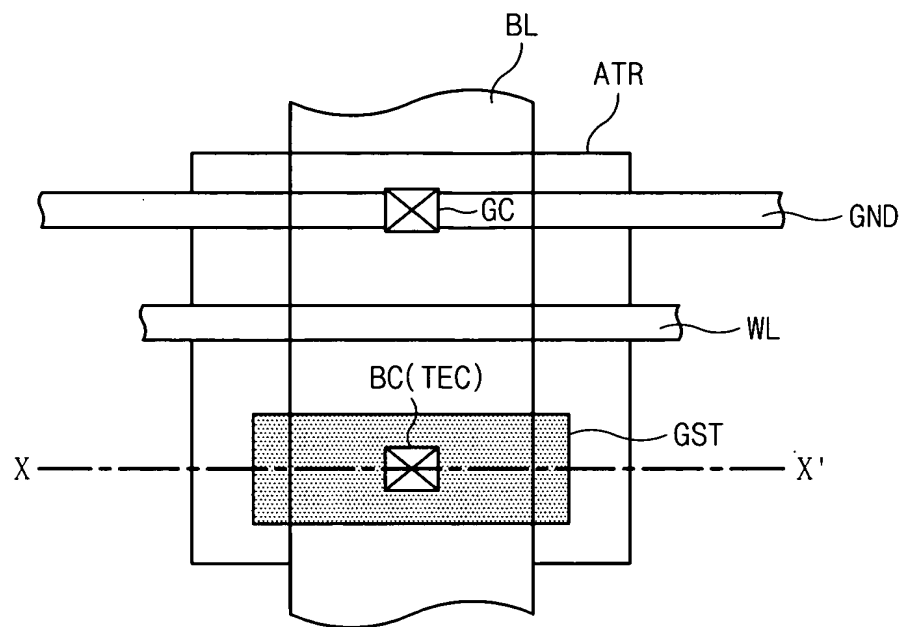


Fig. 2B

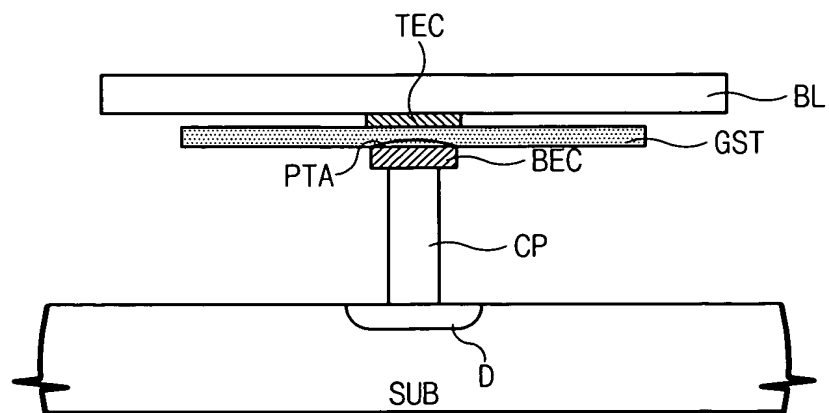


Fig. 3

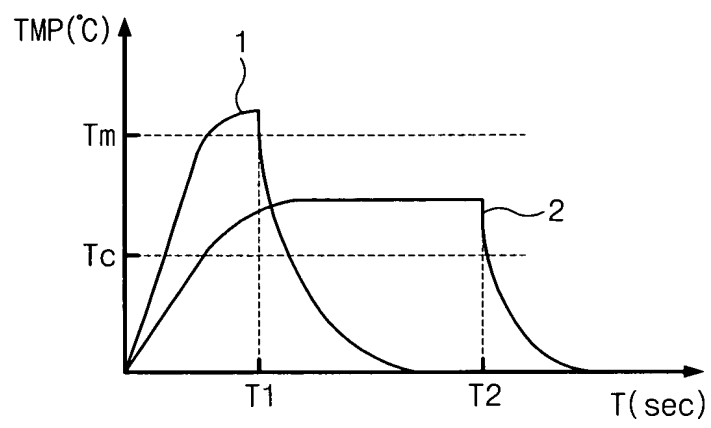


Fig. 4

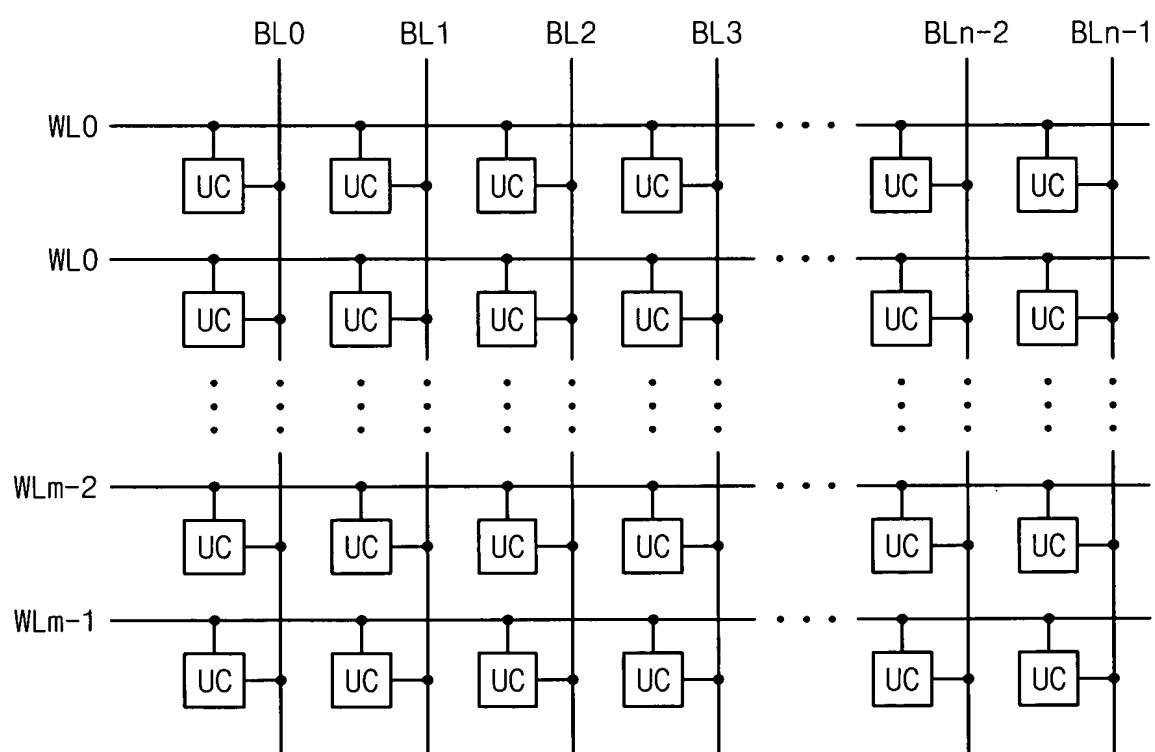


Fig. 5

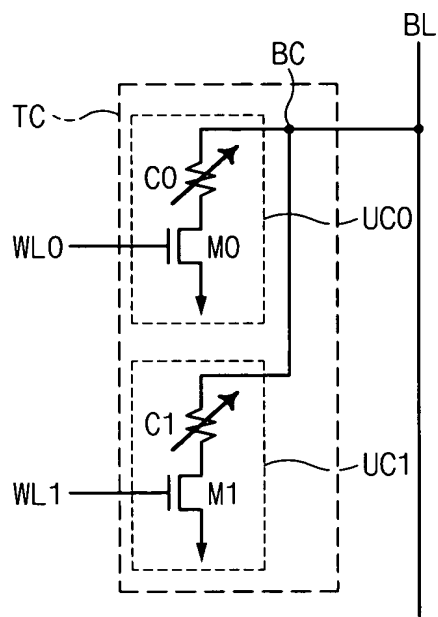


Fig. 6

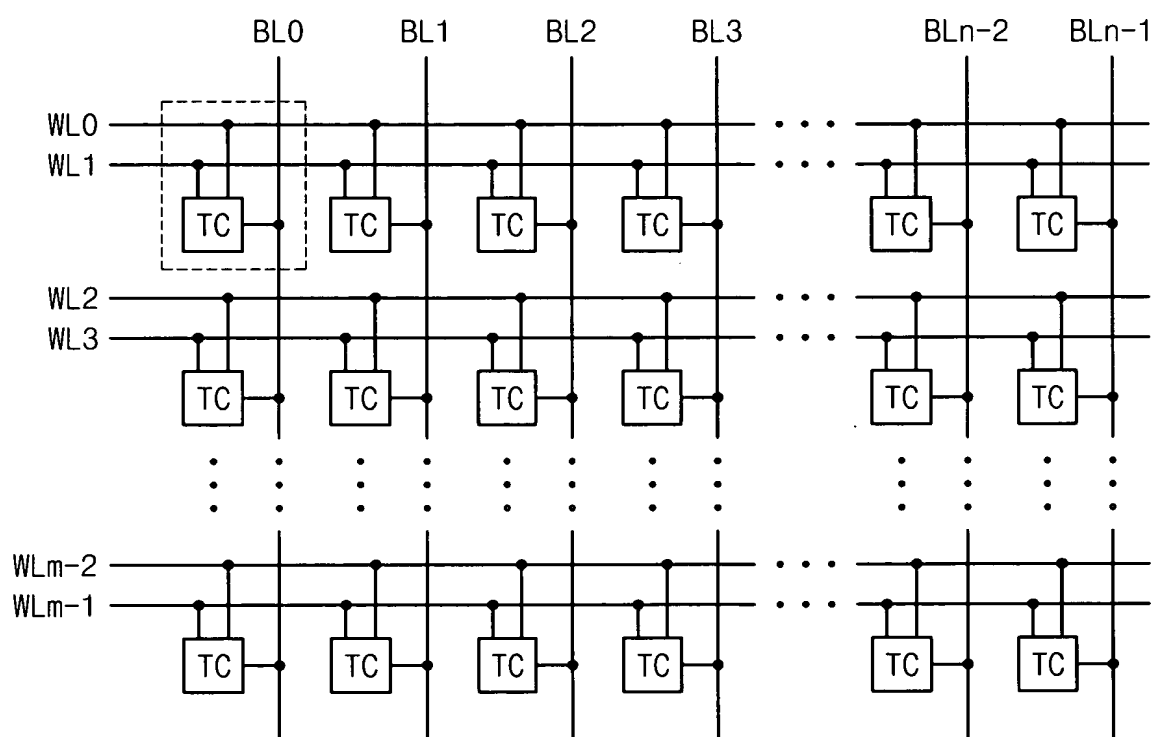


Fig. 7

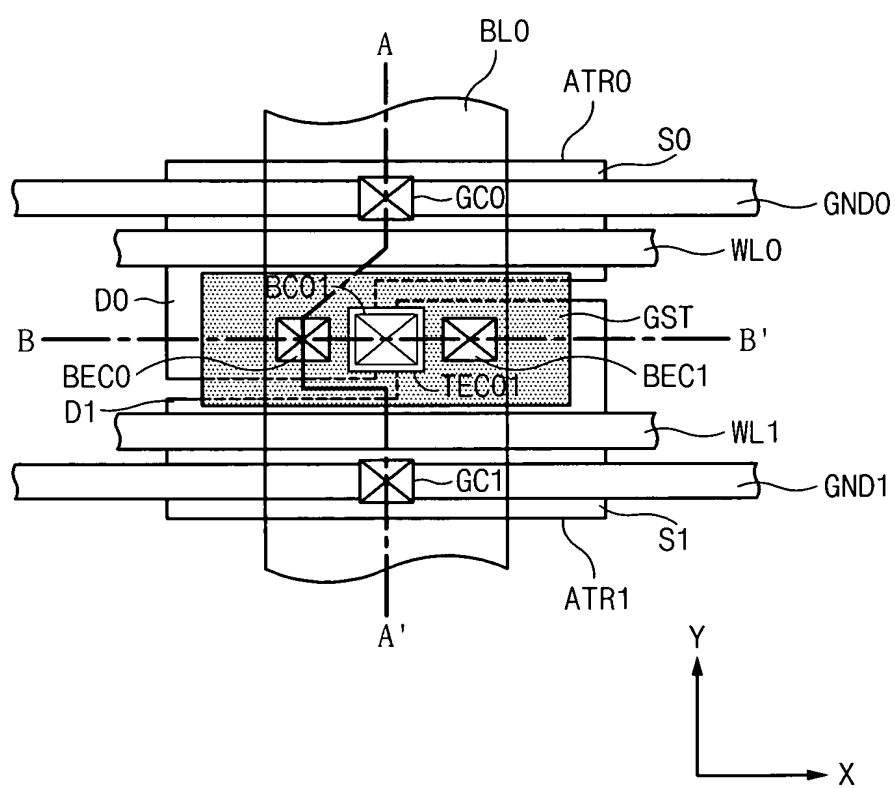


Fig. 8A

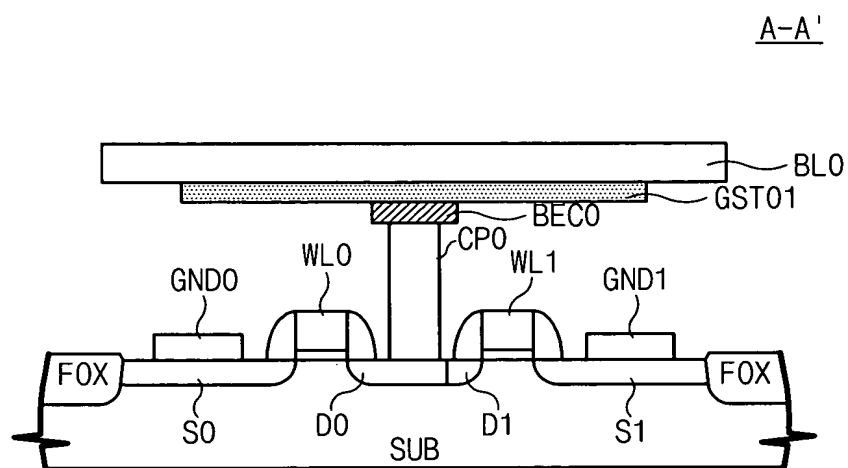


Fig. 8B

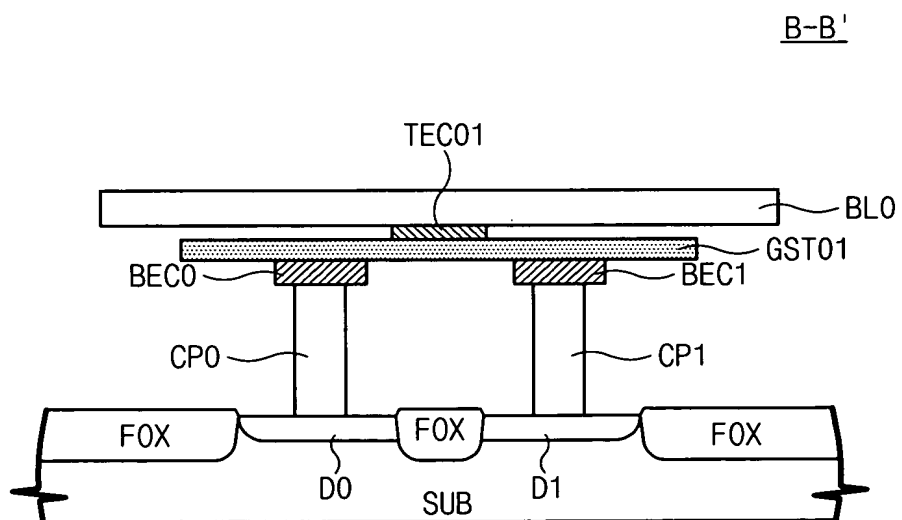




Fig. 9

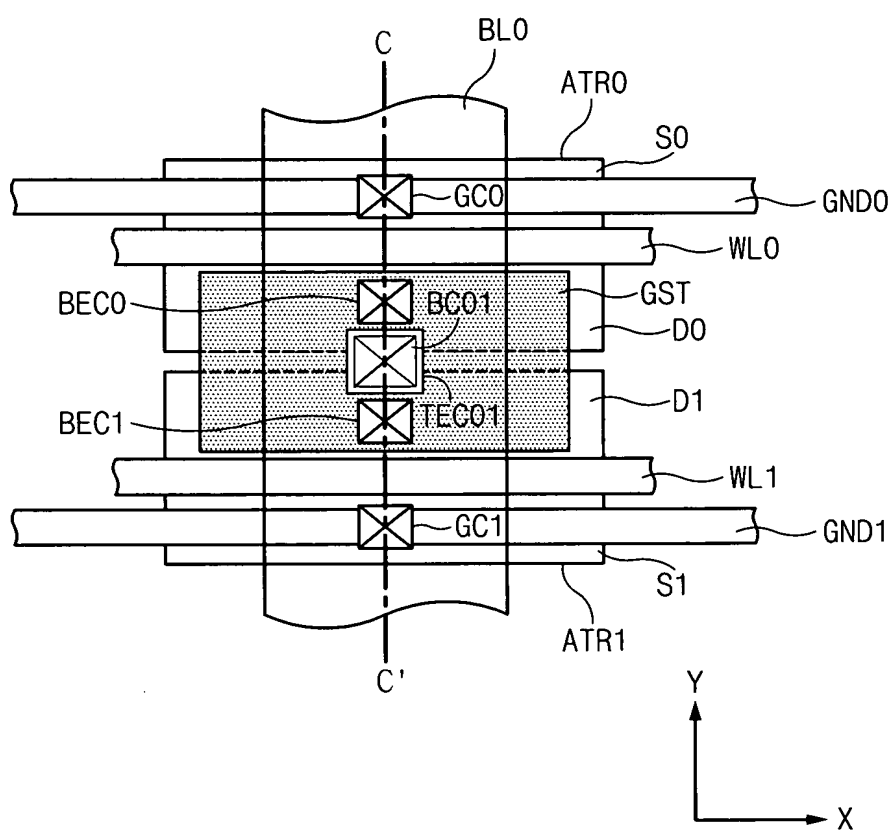


Fig. 10

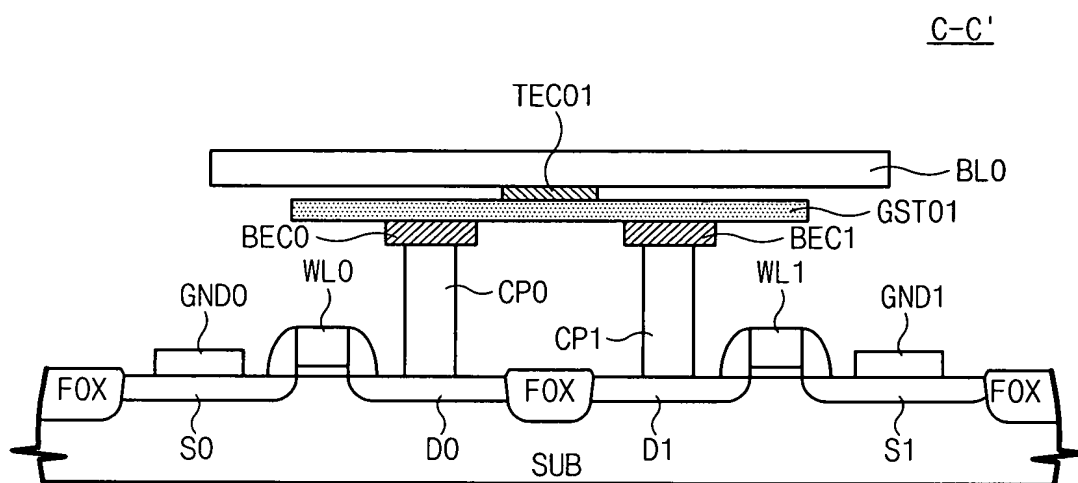


Fig. 11

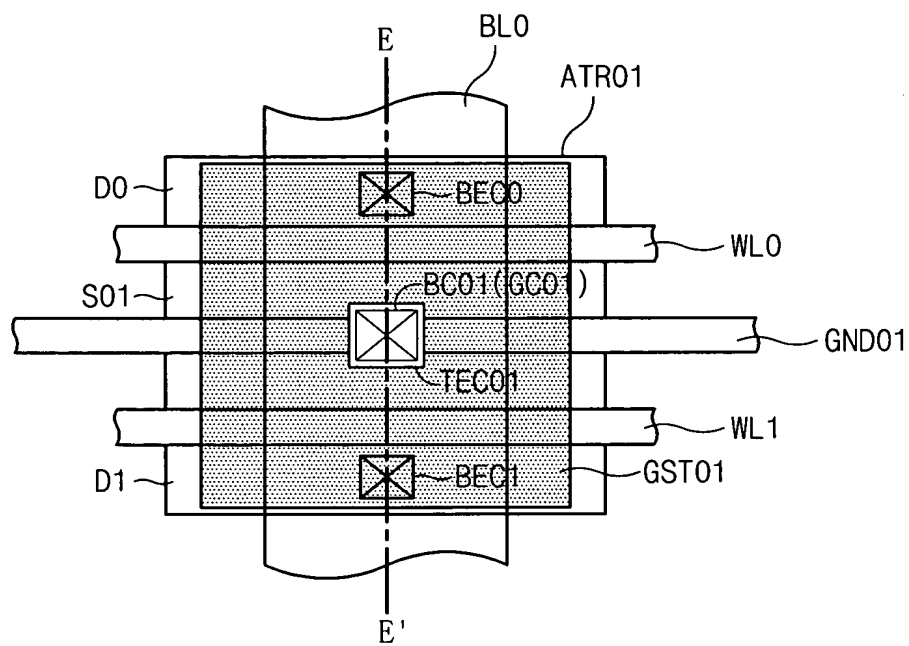


Fig. 12

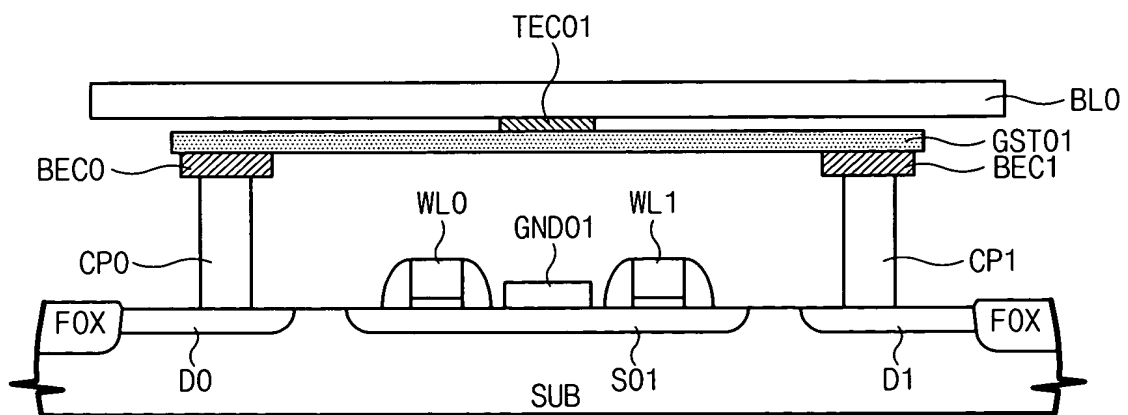


Fig. 13A

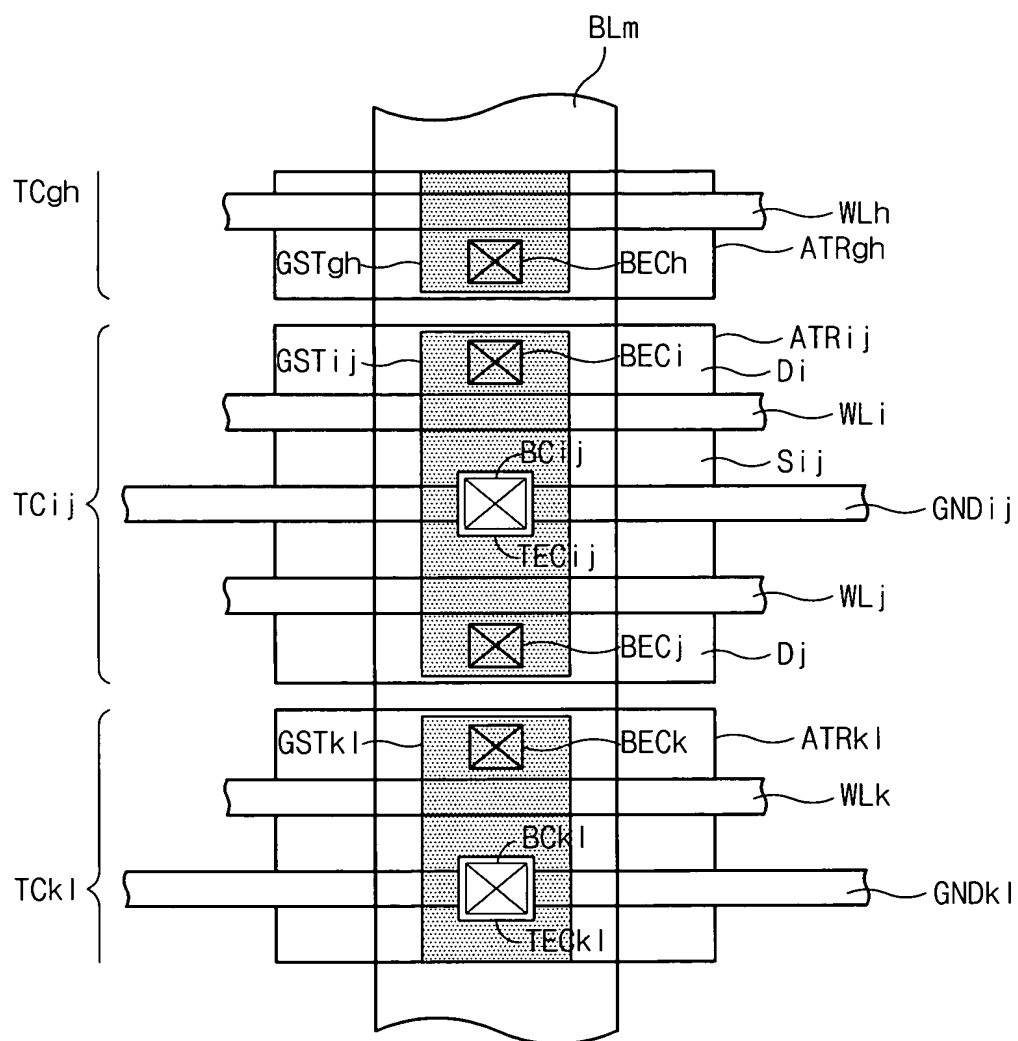


Fig. 13B

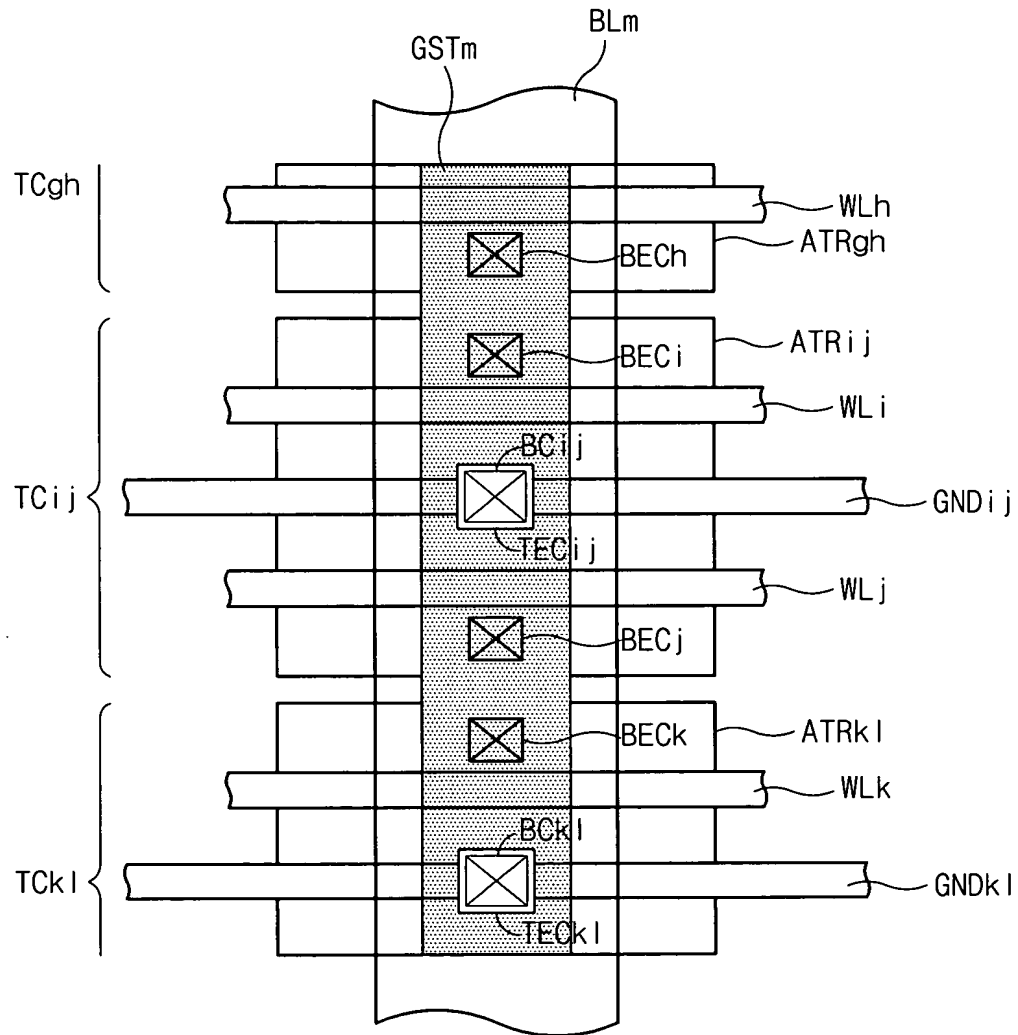
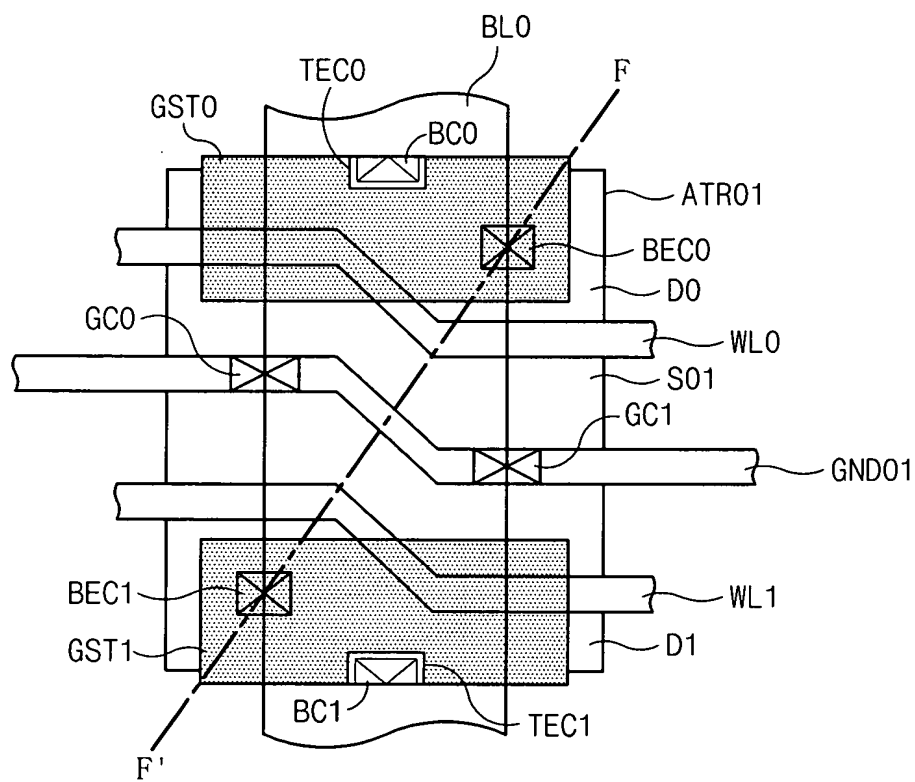
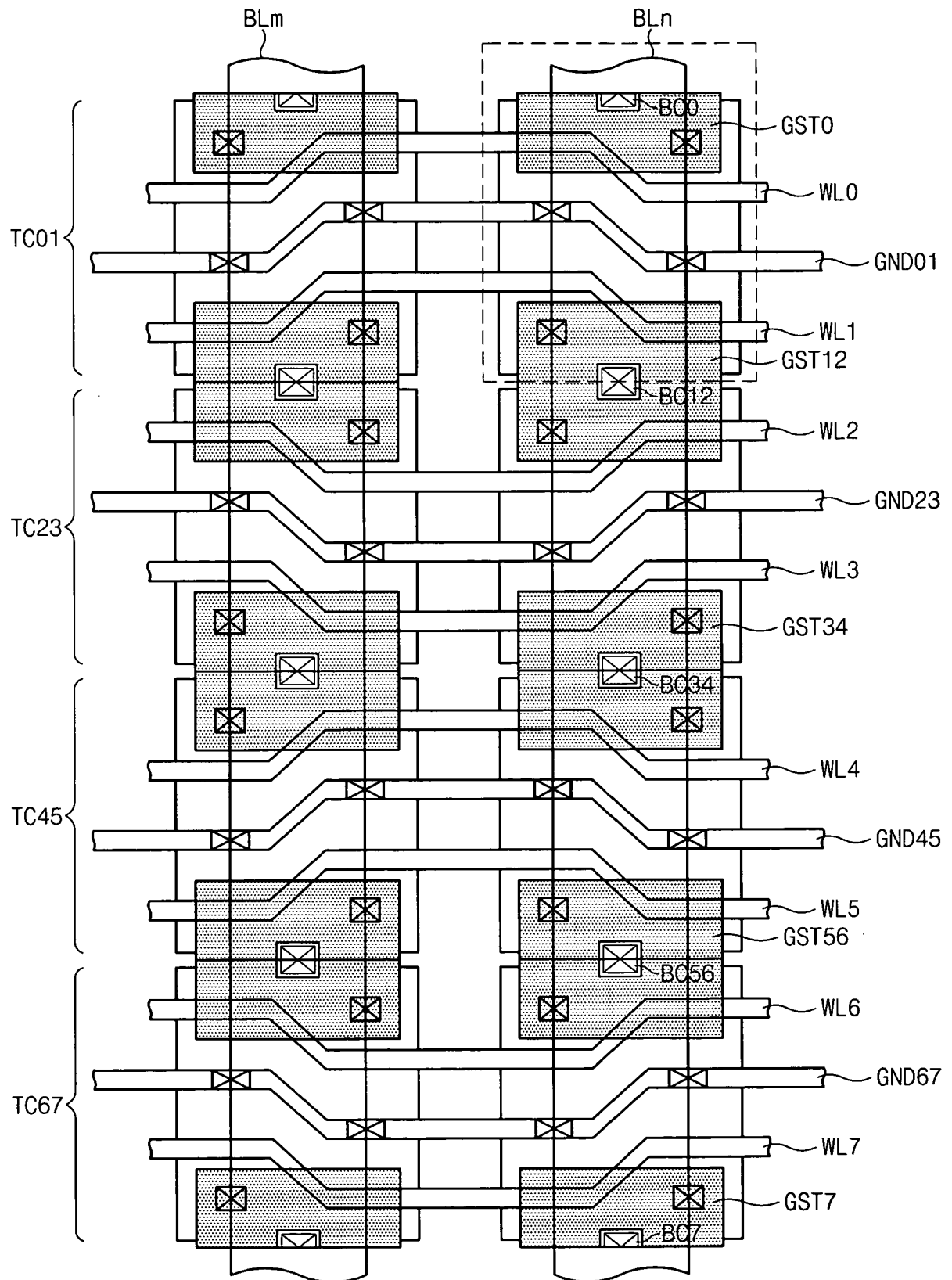


Fig. 14



A cross-sectional view of a semiconductor device. The substrate is labeled SUB. On the left, there is a memory cell D0 consisting of a FOX layer, a CP0 layer, a BEC0 layer, and a GST0 layer. In the center, there is an access region S01 containing three gates: WL0, GND01, and WL1. On the right, there is another memory cell D1 consisting of a FOX layer, a CP1 layer, a BEC1 layer, and a GST1 layer.

Fig. 16





A detailed cross-sectional view of a semiconductor device, likely a 3D NAND memory array. The structure is divided into two main horizontal sections, labeled '0' and '1', representing different memory cells or word lines. The top section (0) includes a bit line (BL0) at the top, followed by a tunneling layer (TEC0), a barrier layer (BC0), and a gate stack (GST0). Below these are a word line (WL0) and a gate (GC0). The bottom section (1) includes a bit line (BL1) at the bottom, followed by a tunneling layer (TEC1), a barrier layer (BC1), and a gate stack (GST1). Above these are a word line (WL1) and a gate (GC1). The device is surrounded by a substrate (GND01) and a top layer (ATR01). Various other layers and gates are labeled, including BEC0, BEC1, and ATR01. The diagram shows the complex layering and alignment of these components in a 3D structure.

Fig. 18

